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(54) Wide frequency range VCO with low jitter

(57) Each starved-inverter of a voltage controlled ring oscillator has an output transfer gate associated therewith. The pair of complementary switches (MTP,MTN) composing a transfer gate being controlled in common with the relative current generators of the starved-inverter stage, by the frequency control voltage (Vc) and by the voltage difference between the supply voltage and the control voltage (Vdd-Vc), respectively.

The frequency produced by the oscillator is linearly proportional to the control voltage (Vc) and inversely proportional to the square root of the supply voltage (Vdd), for an enhanced noise immunity and improved frequency stability.

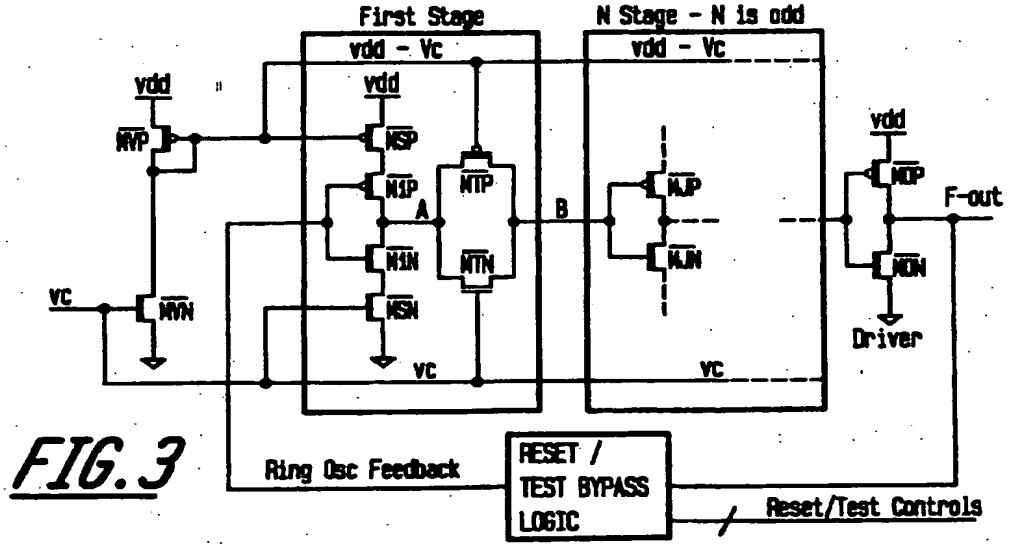

FIG. 3

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Description

The present invention relates to a voltage controlled ring oscillator (VCO) with a wide frequency range and enhanced noise immunity, particularly suited for implementing phase locked (PLL) control systems.

Phase locked loop systems (PLLs) are often integrated in VLSI devices, typically in integrated circuits for specific applications (ASICs) microprocessors, and the like.

PLLs are often used as frequency synthesizers capable of generating square wave frequencies that may vary from 10 to over 200 MHz starting from an input clock signal with a frequency commonly comprised between 1 and 4 MHz.

PLLs are also used for square shaping or reshaping clock signals, for recovering digital data, etc.. Whichever the type of application, PLLs must have a short term instability of the output frequency (output jitter) as low as possible. In other words, they must be highly immune to causes of short term instabilities, in other words, to high frequency noise.

The presence of a marked jitter is highly detrimental in VLSI applications because the output square wave produced by the PLL system has a degree of uncertainty of the rise and fall fronts, which if used as system clock signal may negatively affect system's because of a reduction of the time-scale margins for a correct handling of data and of the data retention time.

Very often PLL systems must ensure a maximum instability of the switching fronts of the output signal below about 0.5 ns, notwithstanding the fact that they must function in a relatively noisy "environment".

Short term instability (jitter) in VCO, realized in VLSI CMOS technology, is primarily caused by the high frequency noise that is generated within the integrated circuit and which is injected in the VCO of a PLL through the supply rails, as well as through the control voltage (Vc) line of the output frequency generated by the VCO.

A block diagram of a frequency synthesizer based on a PLL employing a voltage controlled oscillator (VCO) is depicted in Fig. 1.

Notwithstanding that the behavior of a phase locked loop is in some measure similar to that of an adaptive filter and that therefore the long term instabilities of the input clock signal are effectively filtered, short-term instability caused by the noise coming from the supply rails and from the control voltage line remains a difficult problem to be solved, especially in VLSI devices.

Among the circuit blocks that compose a PLL, the phase and frequency comparator (PFD) and the low pass filter are intrinsically immune to short term instabilities, while the frequency divider (1/N) generates negligible jitter as compared with the high frequency noise that is normally present at the output of the VCO clock (Fig.1). Therefore, it may be said that the control of jitter in a PLL may be reconducted to providing a voltage controlled oscillator having a high immunity toward high frequency noise.

Substantially, most of the times in VLSI applications, the VCO employed for implementing a PLL consists of a voltage controlled ring oscillator. A ring oscillator offers a high gain and a great stability in a relatively simple and least burdensome way.

A typical architecture of a VCO is depicted in Fig. 2. The VCO is implemented by a plurality (odd number) of inverting (delay) stages connected in cascade, each commonly being a so-called *starved-inverter* composed of transistors M1, M2, M3 and M4. Each inverting stage is often followed by a Schmitt trigger circuit for providing a partial filtering of short term frequency instabilities.

In a *starved-inverter*, the transistors M1 and M4, controlled by the output signals produced by the voltage-current control converter, act as current sources, while the transistors M2 and M3 work essentially as digital switches by enabling the source and sink currents. Therefore, the node n1 is alternately charged and discharged, thus causing the switching of the output Schmitt trigger (S1) associated with the inverting stage when its triggering thresholds (in the two switching directions) are crossed. The signals propagate through the N inverting stages of the oscillator producing a square wave output signal F_OUT.

Because of the hysteresis toward the input voltage signal switchings, the use of a Schmitt trigger at the output of each inverting stage of the ring oscillator tends to reduce the instability of the switching point of the inverting stage.

However, the noise that is injected through the control voltage line Vc as well as through the supply rails (Vdd and GND), in practice modulates the switching thresholds of the various inverting (delaying) stages that compose the ring oscillator thus causing a jitter of the switching fronts of the output signal.

Moreover, in known VCOs the output frequency varies linearly with the supply voltage and the PSR is intrinsically poor. Furthermore, the frequency produced by the VCO increases with the supply voltage and this makes the transfer function of the PLL (and therefore its stability) strongly dependent on the operating voltage unless effective but costly voltage regulation circuits are implemented. Notwithstanding the use of a Schmitt trigger at the output of each inverting delay stage of the ring oscillator, the amount of noise that is effectively filtered out is relatively modest. In a circuit working at 5V, a PSR of 10%/V is normal in known systems.

There is clearly a need and/or utility for a voltage controlled oscillator (VCO) that, though being based on a ring oscillator architecture, offering a relative intrinsic stability, high gain and sturdiness with a relatively modest and least burdensome circuit complexity, has a markedly reduced sensitivity to supply voltage variations and an enhanced hys-

teresis of each inverting stage so as to ensure a higher rejection of high frequency noise. The circuit should remain easily integratable in CMOS technology.

A method for markedly improving the ability to reject disturbances coming from the supply rails and from the control voltage line of a voltage controlled ring oscillator has now been found and represents an object of the present invention.

Basically the method consists in making the output frequency produced by the oscillator directly proportional to the control voltage and inversely proportional to the square root of the supply voltage. Such an objective may be implemented by employing in place of a Schmitt trigger at the output of each inverting (delaying) stage of the ring oscillator as commonly done in the prior art VCOs, a transfer gate composed of a pair of parallel complementary switches, between the output of each inverting stage and the input of the inverting stage that follows in the chain of cascaded stages and by controlling a switch of the pair constituting the transfer gate in common with the relative current generator of the *starved-inverter* that constitutes the inverting stage by the control voltage and the other switch of the pair and the other current generator by the voltage difference between the supply voltage and the control voltage.

A further advantage deriving from such an embodiment of the invention is that an exceptionally high hysteresis is produced in each inverting stage of the ring oscillator, which may reach up to 80-90% of the supply voltage, thus further increasing high frequency noise rejection ability.

Differently from the known architecture, the voltage controlled oscillator of the invention does not require a voltage-to-current converter for driving a first *starved-inverter* of the chain of inverters. According to the invention, the first inverting stage may be in practice a simple unit gain voltage shifting stage driven directly by the control voltage signal, while all the following inverting (delaying) stages (in an even number) are customarily *starved-inverters*, each followed by a transfer gate.

The different aspects and advantages of the invention will become even more evident through the following description and analysis of an important embodiment and by referring to the annexed drawings, wherein:

Figure 1 is a block diagram of a PLL employing a VCO;
Figure 2 shows the structure of a ring type VCO, according to a known technique;
Figure 3 is a diagram of a voltage controlled ring oscillator made according to the present invention;
Figures 4a and **4b** show the internal voltages of the VCO of the invention according to a simulated operation;
Figure 5 shows characteristic curves of the VCO of the invention simulated for different supply voltages.

Referring to Fig. 3, the VCO's control circuit, responsive to a control voltage signal Vc, basically consists of a first inverting stage in the form of a unit gain voltage shifter, formed by a pair of complementary transistors MVN and MVP.

This voltage shifting stage outputs a voltage difference between the supply voltage Vdd and the control voltage Vc.

The oscillator further comprises a plurality of delaying inverting stages of the so-called *starved-inverter* type, in an even number, an output driver and a control logic circuitry (Reset, Test By-pass Logic) functionally coupled in the feedback line of the ring oscillator. The control logic block may be similar to the control blocks that are normally employed in ring type VCOs for implementing a reset, stop and by-pass function for performing tests on the integrated circuit.

The voltage shifting a stage is preferably made by a pair of complementary transistors MVN and MVD designed so as to have an identical transconductance for ensuring a unit voltage gain. The stage shifts the control voltage Vc so that the following delaying inverting stages cascaded therefrom which form the ring oscillator are controlled in their n-channel sections directly by the control voltage Vc and in their p-channel sections by a voltage difference between the supply voltage and the control voltage (Vdd-Vc).

An output transfer gate composed of a pair of complementary transistors functionally connected in parallel is coupled to the output of each *starved-inverter* delay stage that follows the first inverting stage represented by the unit gain voltage shifter. The *starved-inverter* stages may be in an even number so that the total number of inverters in the reaction loop of the oscillator be odd. The complementary transistors that form each of said output transfer gate are driven in common with the respective current generators of the *starved-inverter* stage to the output of which the transfer gate is associated, namely: by the control voltage Vc for the n-channel section and by the voltage difference Vdd-Vc for the p-channel section, respectively.

With reference to the diagram of Fig. 3, an analysis of the operation of the circuit of the invention is hereinbelow reported. The analysis refers to a first *starved-inverter* stage, that follows the unit gain inverting stage that constitutes the control voltage shifting stage, the load of which is represented by the pair of transistors MjN and MjP of a following *starved-inverter* stage.

As said above, the transistors MVN and MVP that form the inverting control voltage shifting stage (having a unit voltage gain) are designed so as to have the same transconductance, that is:

$$gm_{MVN} = gm_{MVP}$$

This identity of transconductance may be considered verified in the range of variation of electrical parameters due to the process spread and of the operating temperature.

Therefore, in first approximation, MSN and MSP are both biased with a same |VGS|. In fact MSN is biased by the control voltage Vc, while MSP is biased by the difference Vdd-Vc, both referred to ground potential.

The allowed range of variation for the control voltage Vc may be set as:

$$0.25 < Vc/Vdd < 0.66$$

By assuming the node A charged to Vdd, the node B is also charged to Vdd and therefore the transistor M1P is ON while the transistor M1N is OFF.

In these conditions, MTN is OFF and MTP is ON. When the reaction node of the ring oscillator switches, M1N conducts and MSN starts to discharge the node A by a constant current. The voltage on the node B tracks the voltage of the node A.

When:

$$V(A) = V(B) = Vdd - Vc + |V_{TP}| = V1$$

the transistor MTP turns OFF too, thus the node B is practically disconnected from the node A and clamped to the voltage V1. The transistor MSN continues to discharge the node A through a linear voltage ramp.

When:

$$V(A) = Vc - V_{TN} = V2$$

MTN turns ON, the charge distributes itself over the nodes A and B, the voltage V(B) is pulled down toward the voltage V(A) and finally both nodes A and B assume the same potential, which is much lower than the switching threshold of the following inverting stage. Therefore, the following inverting stage (MjT and MjN ...) switches thus propagating the signal through the chain of delaying and inverting stages of the VCO.

The voltage swing of the signal in the first *starved-inverter* stage, before the following inverting stage switches, is therefore equal to Vdd-V2.

It may be demonstrated through similar deductions that when the node A starting from ground potential reaches the voltage Vdd, the clamp voltage V1 is given by:

$$V(A) = V(B) = Vc - V_{TN} = V1$$

while charge distribution takes place when:

$$V(A) = Vdd - Vc + |V_{TP}| = V2;$$

the voltage swing being equal to V2.

In conclusion, the output signal swing of the first *starved-inverter* stage of the oscillator, before the following inverting stage switches, in either direction, (rise and fall of the voltage on the node V(A)) is given by:

$$\Delta V = Vdd - Vc + V_T$$

on account of the assumption that:

$$V_{TN} = |V_{TP}| = V_T$$

The delay of propagation through the N+1 inverting stages that form the reaction loop of the VCO is given by:

$$T_{VCO} = (N+1)C_{load}\Delta V/I_o$$

wherein I_o is the charge/discharge current through MSN and MSP, that is:

$$I_o = \beta(Vc - V_T)^2,$$

$$\text{where } \beta = \beta_{MSN} = \beta_{MSP}$$

considering that MSN and MSP are designed to have the same gain, the output frequency of the VCO is given by:

$$f_{VCO} = 1/2T_{VCO} = \text{const.} \times C_{load}^{-1} \times (Vc-V_T)^2/(Vdd-Vc-V_T)$$

where C_{load} is essentially the drain junction capacitance of M1N, M1P, MTN and MTP. The gate capacitances of transistors MjN and MjP are effectively decoupled from the node A and therefore they do not contribute to C_{load}.

By assuming a step-junction profile, the following expression may be written:

$$C_{drain}(V) = \text{const.} \times (1 - V/\phi)^{-0.5}$$

where ϕ is constant dependent from the fabrication process.

In first approximation, C_{load} corresponds to the above indicated drain capacitance, averaged over ΔV, that is:

$$C_{load} = \text{const.} \times ((1 + \Delta V/\phi)^{0.5} - 1)/Vdd$$

Therefore,

$$f_{VCO} = \text{const.} \times [Vdd/((1 + \Delta V/\phi)^{0.5} - 1)] \times (Vc-V_T)^2/\Delta V$$

By considering the definition of the ΔV parameter, the last equation may be simplified as follows:

$$f_{VCO} = \text{const.} \times Vc/Vdd^{0.5}$$

According to premises, the output frequency produced by the VCO is a linear function of the control voltage Vc, while it varies with Vdd according to an inverse square root function of the supply voltage.

The advantages that are obtained are evident.

- High PSR

To a variation of 10% of Vdd corresponds a variation of just about 3% of the frequency generated by the VCO.

- Large Hysteresis

By assuming for example: Vdd=5V, Vc=2V and V_T=1V, the maximum ΔV excursion that may be reached in CMOS devices may be as large as 4V. Such a large voltage swing tends to minimize short term instability modulation of the output frequency produced by the oscillator (jitter modulation).

- Inverse relationship between the frequency and the supply voltage

This condition helps in stabilizing the loop. In fact, the dependency from Vdd of the gain of the VCO compensates the reduced gain of the phase and frequency detector (PFD) at low Vdd values. This is extremely advantageous by considering that the bandwidth of a PLL depends from the product of the two gains.

The operating parameters of the VCO of Fig. 3, functioning at a nominal supply voltage of 5V are shown as diagrams of the internal voltages in Figures 4a and 4b, and as a transfer characteristics of the oscillator, for a supply voltage of 4.5V, 5.0 and 5.5, respectively, in Fig. 5.

Claims

1. A voltage controlled oscillator (VCO) comprising a plurality of delaying inverting stages connected in cascade and forming a positive feedback loop, each delaying inverting stage being composed of a pair of complementary switches (MjP, NjN) driven in common and a pair of complementary current generators (MSP, MSN), connected between the relative switch (MjP, MjN) and a supply node (Vdd) and a ground node (GDN) of the circuit, respectively, and control means responsive to a control voltage (Vc), characterized by comprising

   a transfer gate composed of a pair of complementary switches connected in parallel (MTP, MTN), functionally coupled to the output of each inverting stage and to the input of the following inverting stage of said plurality of stages connected in cascade;

   each of said complementary switches (MTP, MTN) of each transfer gate being controlled in common with the relative current generator (MSP, MSN) of the inverting stage to the output node of which the transfer gate is coupled;

   a switch and a current generator (MTN, MSN) being controlled by said control voltage (Vc) while the other

switch and current generator (MTP, MSP) being controlled by a voltage difference (Vdd-Vc) between the supply voltage (Vdd) and said control voltage (Vc).

2. The voltage controlled ring oscillator according to claim 1, made in CMOS technology wherein said complementary pairs of switches and current generators are formed by integrated CMOS structures.

3. The voltage controlled ring oscillator according to claim 2, wherein the ratio between said control voltage (Vc) and the supply voltage (Vdd) is comprised between 0.25 and 0.66.

4. The voltage controlled ring oscillator according to claim 1, wherein said control means comprise a unit gain, inverting voltage shifting stage composed of a pair of complementary transistors (MVP, MVN) functionally connected in series between a supply node (Vdd) and a ground node (GDN), the n-channel transistor (MVN) of the pair being driven through a gate thereof by said control voltage (Vc) while a diode-configured p-channel transistor (MVP) of said pair has a gate and a source connected in common to the drain of the n-channel transistor (MVN), constituting a node biased at said difference voltage (Vdd-Vc).

5. The voltage controlled ring oscillator according to claim 4, wherein said transistors (MVN, MVP) of the pair have identical transconductance.

6. A method for reducing short term instability of the output frequency produced by a voltage controlled ring oscillator due to noise coming from the supply rails (Vdd, GDN) and from the control voltage line (Vc), characterized by making the frequency produced by the oscillator linearly proportional to the control voltage (Vc) and inversely proportional to the square root of the supply voltage (Vdd).

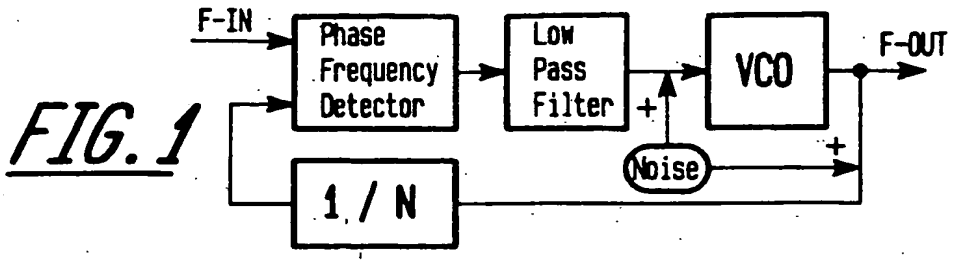

FIG. 1

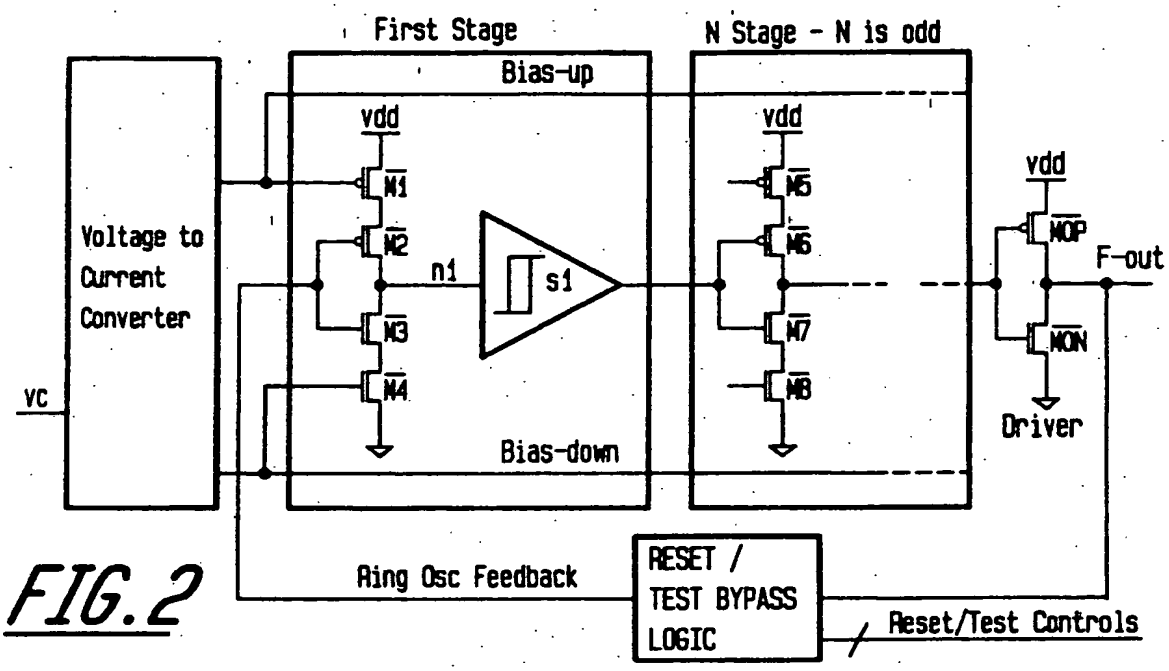

FIG. 2

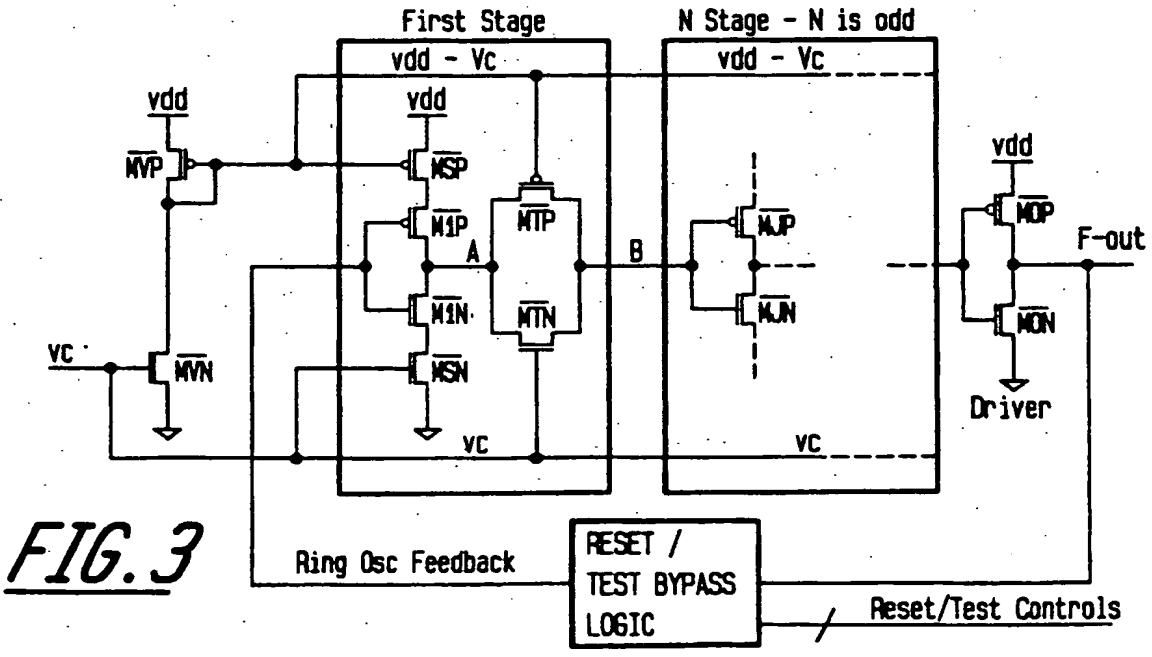

FIG. 3

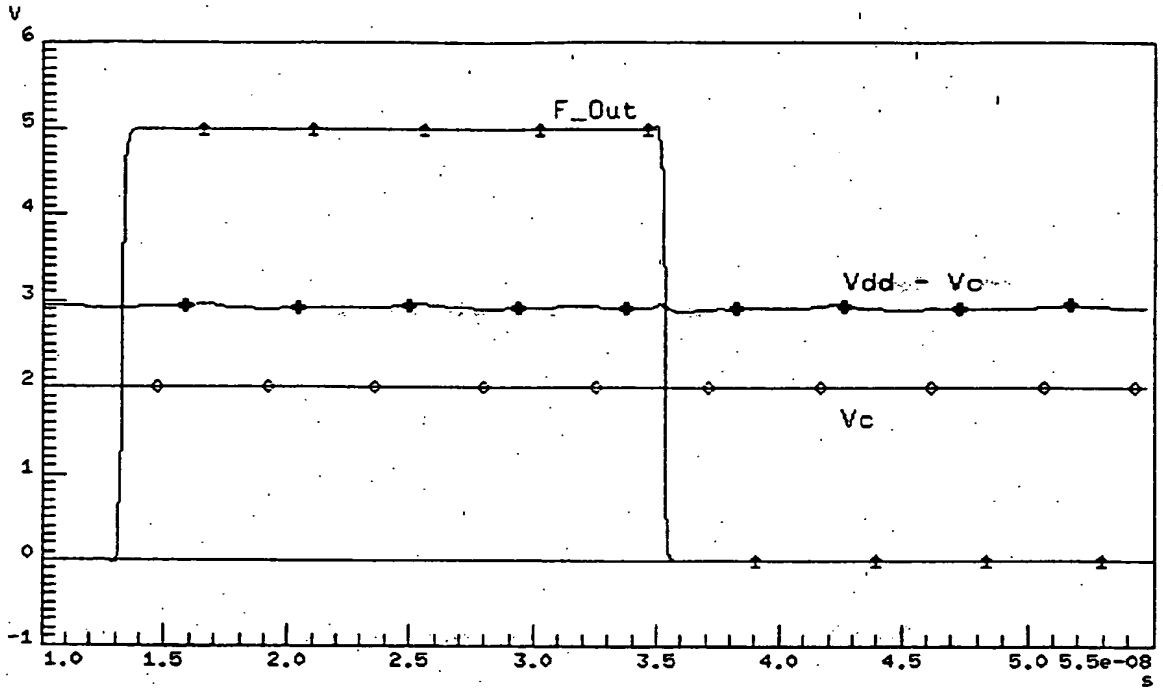

FIG. 4a

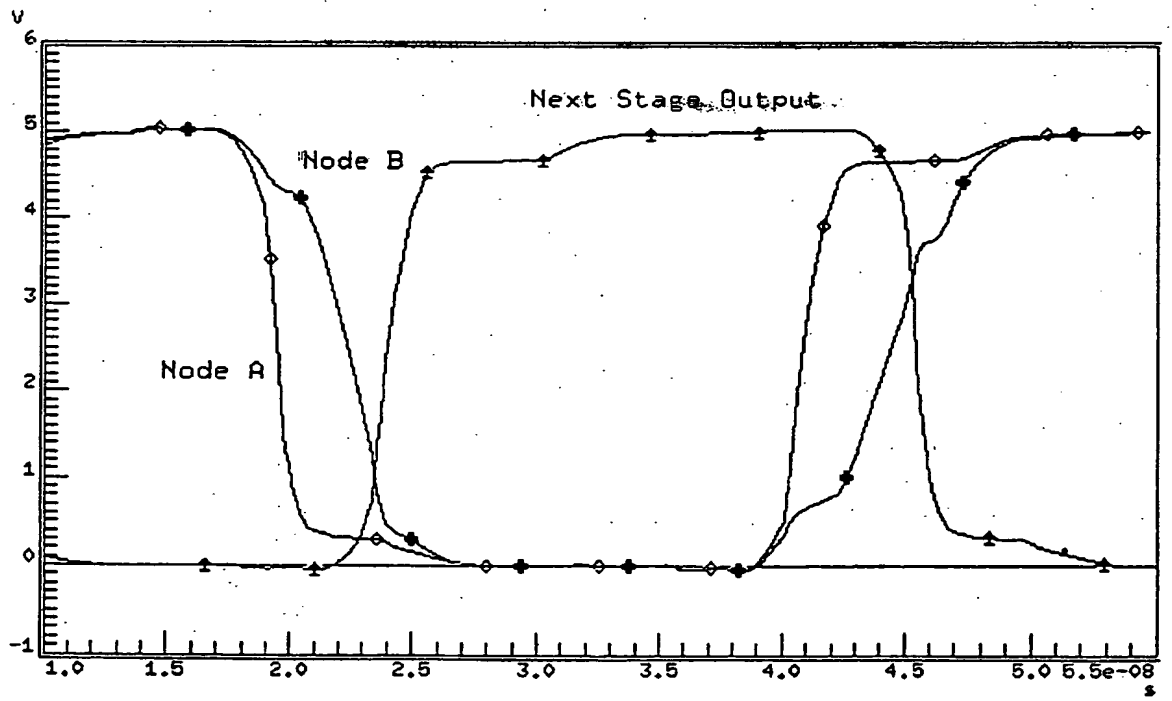

FIG. 4b

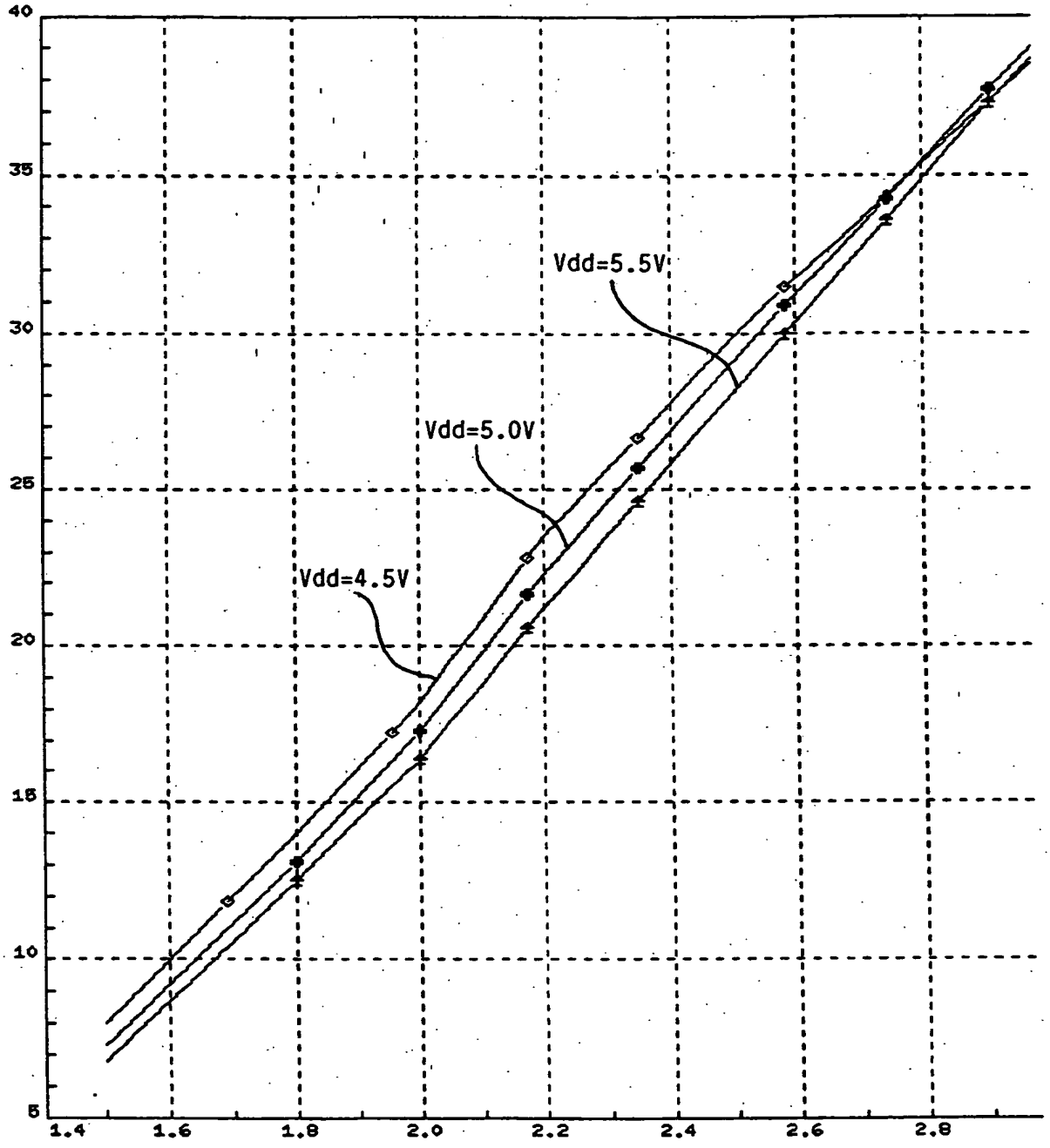

FIG. 5

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EUROPEAN SEARCH REPORT

Application Number
EP 95 83 0081

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US-A-5 285 483 (OGAWA ET AL.) * column 5, line 37 - column 6, line 9; figure 2 *	1,2,4	H03K3/03 H03K3/354
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS., vol.27, no.7, July 1992, NEW YORK US pages 1073 - 1079 SCHUSTER ET AL. 'On-chip test circuitry for a 2-ns cycle, 512-kb CMOS ECL SRAM' * page 1077, left column, line 10 - line 40; figure 7 *	1,2	
A	NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, SECTION - A: ACCELERATORS, SPECTROMETERS, DETECTORS AND ASSOCIATED EQUIPMENT, vol.305, no.3, 1 August 1991, AMSTERDAM NL pages 541 - 548 VANSTRAELEN ET AL. 'Design implications of a p-well CMOS technology for the realization of monolithic integrated pixel arrays' * page 545, left column, line 4 - right column, line 2; figure 4 *	1,2	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H03K H03L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 August 1995	Cantarelli, R

CATEGORY OF CITED DOCUMENTS

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